1. (original) A clock divider for a DLL (Delay Lock Loop) circuit of a synchronous memory device for synchronization of an external input clock with an internal input clock, the clock divider comprising:

M (where M is an integer that is larger than 2) dividers connected in series; and

a power-down controller for receiving an output signal of the (M-l)-th divider and an output signal of the M-th divider, and selectively outputting the output signals;

wherein the respective dividers divide a frequency of a clock signal inputted to the respective dividers into 1/2.

2. (original) The clock divider as claimed in claim 1, wherein the output signal of the power-down controller has a frequency obtained by dividing the frequency of the clock signal inputted to the first divider into $\frac{1}{2}^{M}$ or $\frac{1}{2}^{(M-1)}$ in accordance with a logic level of a control signal.

3. (original) The clock divider as claimed in claim 2, wherein if the logic level of the control signal is a first state (high level) , the output signal of the power-down controller becomes the output of the (M-l)-th divider, and if the logic level of the control signal is a second state (low level), the output signal of the power-down controller becomes the output of the M-th divider.

4. (original) The clock divider as claimed in claim 3, wherein the control signal is a clock enable signal used in the synchronous memory device.

5. (currently amended) The clock divider as claimed in ~~anyone of claims~~ claim 1 ~~to 4~~, wherein a pulse width of a high-level state of the output signal of the first divider is the same as a period of the input signal of the first divider, and a pulse width of a low-level state of output signals of the second to M-th dividers is the same as the period of the input signal of the first divider.

6. (currently amended) The clock divider as claimed in claim 4 ~~6~~, wherein the power-down controller comprises two transmission gates, and the two transmission gates are selectively turned on/off according to the control signal.

7. (original) A clock dividing method for a DLL (Delay Lock Loop) circuit of a synchronous memory device for synchronization of an external input clock with an internal input clock, the method comprising the steps of:

selectively outputting an output signal of a (M-1)th divider and an output signal of an M-th divider among M dividers, connected in series, for respectively dividing a frequency of the input clock signal into 1/2.

Please add the following new Claims 8-12:

8. (New) The clock divider as claimed in claim 2 wherein a pulse width of a high-level state of the output signal of the first divider is the same as a period of the input signal of the fiLst divider, and a pulse width of a low-level state of output signals of the second to M-th dividers is the same as the period of the input signal of the first divider.

9. (New) The clock divider as claimed in claim 8, wherein the power-down controller comprises two transmission gates, and the two transmission gates are selectively turned on/off according to the control signal.

10. (New) The clock divider as claimed in claim 3 wherein a pulse width of a high-level state of the output signal of the first divider is the same as a period of the input signal of the first divider, and a pulse width of a low-level state of output signals of the second to M-th dividers is the same as the period of the input signal of the first divider.

11. (New) The clock divider as claimed in claim 10, wherein the power-down controller comprises two transmission gates, and the two transmission gates are selectively turned on/off according to the control signal.

12. (New) The clock divider as claimed in claim 4 wherein a pulse width of a high-level state of the output signal of the first divider is the same as a period of the input signal of the first divider, and a pulse width of a low-level state of output signals of the second to M-th dividers is the same as the period of the input signal of the first divider.